CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A processing element having support for alignment of significants, comprising:

a first register block, said first register block including at least one first register for holding a first exponent and a first significant of a first floating point number;

a second register block, said second register block including at least one second register for holding a second exponent and a second significant of a second floating point number and a second logic, said second logic capable of right shifting the significant of the second floating point number and said second logic also being capable of setting to zero each bit in a portion of said second significant to zeros;

a shift control register;

an arithmetic logic unit coupled to said first register block, said second register block, and said shift control register, said arithmetic logic unit storing in the shift control register a value equal to the difference between said first exponent and said second exponent, said arithmetic logic unit causing the second logic to right shift the

significant or set to zero each bit in the portion of the significant, based upon the contents of said shift control register.

2. The processing element of claim 1, wherein the second logic is capable of right shifting the second significant by 2^N bits, wherein N is an integer which ranges from zero to M, where M is a positive integer of at least 3.

3. The processing element of claim 2, wherein if bit J of said shift control register is equal to one, and if J is greater than M+1, the portion corresponds to the 2^J most significant bits of said second significant, and said arithmetic logic unit causes the second logic to set to zero each bit in said portion, or if the second significant is less than 2^J bits, the arithmetic logic unit causes the second logic to set to zero each bit of said second significant.

4. The processing element of claim 2, wherein if bit J of said shift control register is equal to one, and if J is equal to M+1, the arithmetic logic unit causes the second logic to twice right shift said second significant by 2^M bits;

5. The processing element of claim 2, wherein if bit J of said shift control register is equal to one, and if J is less than or equal to M, the arithmetic logic unit causes the second logic to right shift said second significant by 2^J bits.

6. The processing element of claim 2, where if bit J of said shift control register is equal to one,

if J is greater than M+1, then the portion corresponds to the 2^J most significant bits of said second significant, and said arithmetic logic unit causes the second logic to set to zero each bit in said portion, or if the second significant is less than 2^J bits, the arithmetic logic unit causes the second logic to set to zero each bit of said second significant; or

if J is equal to M+1, the arithmetic logic unit causes the second logic to twice right shift said second significant by 2^M bits; or

if J is less than or equal to M, the arithmetic logic unit causes the second logic to right shift said second significant by 2^J bits.

7. The processing element of claim 6, wherein M is equal to 3.

8. The processing element of claim 7, wherein J is equal to 0.

9. The processing element of claim 7, wherein J is equal to 1.

10. The processing element of claim 7, wherein J is equal to 2.

11. The processing element of claim 7, wherein J is equal to 3.

12. The processing element of claim 7, wherein J is equal to 4.

13. The processing element of claim 7, wherein J is equal to 5.

14. The processing element of claim 7, wherein J is equal to 6.

15. The processing element of claim 7, wherein J is equal to 7.

16. The processing element of claim 1, wherein if the value is negative, the arithmetic logic unit causes the content of said first register block to be exchanged with the content of said second register block, and the arithmetic logic unit negatives the value before storing the value in the shift control register.

17. A massively parallel processing system, comprising:

a main memory;

an array of processing elements, each processing element of the array being coupled to said main memory and other processing elmeents of said array, wherein each of said processing elements comprises,

a first register block, said first register block including at least one first register for holding a first exponent and a first significant of a first floating point number;

a second register block, said second register block including at least one second register for holding a second exponent and a second significant of a second floating point number and a second logic, said second logic capable of right shifting the significant of the second floating point number and said second

logic also being capable of setting to zero each bit in a portion of said second significant to zeros;

a shift control register;

an arithmetic logic unit coupled to said first register block, said second register block, and said shift control register, said arithmetic logic unit storing in the shift control register a value equal to the difference between said first exponent and said second exponent, said arithmetic logic unit causing the second logic to right shift the significant or set to zero each bit in the portion of the significant, based upon the contents of said shift control register.

18. The massively parallel processing system of claim 17, wherein the second logic is capable of right shifting the second significant by 2^N bits, wherein N is an integer which ranges from zero to M, where M is a positive integer of at least 3.

19. The massively parallel processing system of claim 18, wherein if bit J of said shift control register is equal to one, and if J is greater than M+1, the portion corresponds to the 2^J most significant bits of said second significant, and said arithmetic logic unit causes the second logic to set to zero each bit in said portion, or if the second significant is less than 2^J bits, the arithmetic logic unit causes the second logic to set to zero each bit of said second significant.

20. The massively parallel processing system of claim 18, wherein if bit J of said shift control register is equal to one, and if J is equal to M+1, the arithmetic logic unit causes the second logic to twice right shift said second significant by 2^M bits;

21. The massively parallel processing system of claim 18, wherein if bit J of said shift control register is equal to one, and if J is less than or equal to M, the arithmetic logic unit causes the second logic to right shift said second significant by 2^J bits.

22. The massively parallel processing system of claim 18, where if bit J of said shift control register is equal to one,

if J is greater than M+1, then the portion corresponds to the 2^J most significant bits of said second significant, and said arithmetic logic unit causes the second logic to set to zero each bit in said portion, or if the second significant is less than 2^J bits, the arithmetic logic unit causes the second logic to set to zero each bit of said second significant; or

if J is equal to M+1, the arithmetic logic unit causes the second logic to twice right shift said second significant by 2^M bits; or

if J is less than or equal to M, the arithmetic logic unit causes the second logic to right shift said second significant by 2^J bits.

23. The massively parallel processing system of claim 18, wherein M is equal to 3.

24. The massive parallel processing system of claim 23, wherein J equals 0.

25. The massive parallel processing system of claim 23, wherein J equals 1.

26. The massive parallel processing system of claim 23, wherein J equals 2.

27. The massive parallel processing system of claim 23, wherein J equals 3.

28. The massive parallel processing system of claim 23, wherein J equals 4.

29. The massive parallel processing system of claim 23, wherein J equals 5.

30. The massive parallel processing system of claim 23, wherein J equals 6.

31. The massive parallel processing machine of claim 23, wherein J equal 7.

32. The massively parallel processing system of claim 17, wherein if the value is negative, the arithmetic logic unit causes the content of said first register block to be exchanged with the content of said second register block, and the arithmetic logic unit negatives the value before storing the value in the shift control register.

33. In a processing element having a first register block including at least one first register for holding a first exponent and a first significant of a first floating point number and a second register block including at least one second register for holding a

second exponent and a second significant of a second floating point number, the processing element having a second logic for right shifting the second significant by 2^N bits, wherein N is an integer ranging from zero to M, wherein M is an integer of at least 3, a method for aligning the second significant, said method comprising the steps of:

(a) storing in a storage control register, a value, said value being equal to second exponent register subtracted from the first exponent register;

(b) for an integer J ranging from 0 to one less than the width of said shift control register in bits, if bit J of the storage control register equals one, and

(1) if J is greater than M+1, setting each bit in the 2^J most significant bits of said second significant to zero, or setting each bit in the second significant to zero if said second significant is less than 2^J bits;

(2) if J is equal to M+1, twice right shifting said second significant by 2^M bits; or,

(3) if J is equal to or less than M, right shifting said second significant by 2^J bits.

34. The method of claim 33, further comprising the step of:

before step (a), if the value is a negative number, exchanging the contents of said first register block with said second register block; and

negativing the contents of the storage control register.

35. The method of claim 33, wherein M is equal to 3.

36. The method of claim 35, wherein J is equal to 7.